Digital Electronics

Multiple Choice Questions and Answers:-

1. Any number with an exponent of zero is equal to:

A.zero

B.one

C.that number

D.ten

Answer: Option B

2. In the decimal numbering system, what is the MSD?

A.The middle digit of a stream of numbers

B.The digit to the right of the decimal point

C.The last digit on the right

D.The digit with the most weight

Answer: Option D

3. Which of the following statements does NOT describe an advantage of digital technology?

A.The values may vary over a continuous range.

B.The circuits are less affected by noise.

C.The operation can be programmed.

D.Information storage is easy.

Answer: Option A

4. The generic array logic (GAL) device is _____.

A.one-time programmable

B.reprogrammable

C.a CMOS device

D.reprogrammable and a CMOS device

Answer: Option B

5. The range of voltages between VL(max) and VH(min) are _____.

A.unknown

B.unnecessary

C.unacceptable

D.between 2 V and 5 V

Answer: Option C

6. What is a digital-to-analog converter?

A.It takes the digital information from an audio CD and converts it to a usable form.

B.It allows the use of cheaper analog techniques, which are always simpler.

C.It stores digital data on a hard drive.

D.It converts direct current to alternating current.

Answer: Option A

7. What are the symbols used to represent digits in the binary number system?

A.0,1

B.0,1,2

C.0 through 8

D.1,2

Answer: Option A

8. A full subtracter circuit requires _____.

A.two inputs and two outputs

B.two inputs and three outputs

C.three inputs and one output

D.three inputs and two outputs

Answer: Option D

9. The output of an AND gate is LOW _____.

A.all the time

B.when any input is LOW

C.when any input is HIGH

D.when all inputs are HIGH

Answer: Option B

10. Give the decimal value of binary 10010.

A.610

B.910

C.1810

D.2010

Answer: Option C

11. Parallel format means that:

A.each digital signal has its own conductor.

B.several digital signals are sent on each conductor.

C.both binary and hexadecimal can be used.

D.no clock is needed.

Answer: Option A

12. A decoder converts _____.

A.noncoded information into coded form

B.coded information into noncoded form

C.HIGHs to LOWs

D.LOWs to HIGHs

Answer: Option B

13. A DAC changes _____.

A.an analog signal into digital data

B.digital data into an analog signal

C.digital data into an amplified signal

D.none of the above

Answer: Option B

14. The output of a NOT gate is HIGH when _____.

A.the input is LOW

B.the input is HIGH

C.the input changes from LOW to HIGH

D.voltage is removed from the gate

Answer: Option A

15. The output of an OR gate is LOW when _____.

A.all inputs are LOW

B.any input is LOW

C.any input is HIGH

D.all inputs are HIGH

Answer: Option A

16. Which of the following is not an analog device?

A.Thermocouple

B.Current flow in a circuit

C.Light switch

D.Audio microphone

Answer: Option C

17. A demultiplexer has _____.

A.one data input and a number of selection inputs, and they have several outputs

B.one input and one output

C.several inputs and several outputs

D.several inputs and one output

Answer: Option A

18. A flip-flop has _____.

A.one stable state

B.no stable states

C.two stable states

D.none of the above

Answer: Option C

19. Digital signals transmitted on a single conductor (and a ground) must be transmitted in:

A.slow speed.

B.parallel.

C.analog.

D.serial.

Answer: Option D

20. In a certain digital waveform, the period is four times the pulse width. The duty cycle is _____.

A.0%

B.25%

C.50%

D.100%

Answer: Option B

21. Select the statement that best describes the parity method of error detection:

A.Parity checking is best suited for detecting double-bit errors that occur during the transmission of codes from one location to another.

B.Parity checking is not suitable for detecting single-bit errors in transmitted codes.

C.Parity checking is best suited for detecting single-bit errors in transmitted codes.

D.Parity checking is capable of detecting and correcting errors in transmitted codes.

Answer: Option C

22. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a(n):

A.Ex-NOR gate

B.OR gate

C.Ex-OR gate

D.NAND gate

Answer: Option A

23. A logic circuit that provides a HIGH output if one input or the other input, but not both, is HIGH, is a(n):

A.Ex-NOR gate

B.OR gate

C.Ex-OR gate

D.NAND gate

Answer: Option C

24. Identify the type of gate below from the equation

A.Ex-NOR gate

B.OR gate

C.Ex-OR gate

D.NAND gate

Answer: Option C

25. How is odd parity generated differently from even parity?

A.The first output is inverted.

B.The last output is inverted.

Answer: Option B

26. Parity systems are defined as either_____ or _____ and will add an extra _____ tothe digital information being transmitted.

A.positive, negative, byte

B.odd, even, bit

C.upper, lower, digit

D.on, off, decimal

Answer: Option B

27. Which type of gate can be used to add two bits?

A.Ex-OR

B.Ex-NOR

C.Ex-NAND

D.NOR

Answer: Option A

28. Why is an exclusive-NOR gate also called an equality gate?

A.The output is false if the inputs are equal.

B.The output is true if the inputs are opposite.

C.The output is true if the inputs are equal.

Answer: Option C

29. Show from the truth table how an exclusive-OR gate can be used to invert the data on one input if the other input is a special control function.

A.Using A as the control, when A = 0, X is the same as B. When A = 1, X is the same as B.

B.Using A as the control, when A = 0, X is the same as B. When A = 1, X is the inverse of B.

C.Using A as the control, when A = 0, X is the inverse of B. When A = 1, X is the same as B.

D.Using A as the control, when A = 0, X is the inverse of B. When A = 1, X is the inverse of B.

Answer: Option B

30. Determine odd parity for each of the following data words:

1011101 11110111 1001101

A.P = 1, P = 1, P = 0

B.P = 0, P = 0, P = 0

C.P = 1, P = 1, P = 1

D.P = 0, P = 0, P = 1

Answer: Option D

31. In a flash analog-to-digital converter, the output of each comparator is connected to an input of a _____.

A.decoder

B.priority encoder

C.multiplexer

D.demultiplexer

Answer: Option B

32.Which term applies to the maintaining of a given signal level until the next sampling?

A.Holding

B.Aliasing

C.Shannon frequency sampling

D."Stair-stepping"

Answer: Option A

33. An op-amp has very _____.

A.high voltage gain

B.high input impedance

C.low output impedance

D.all of the above

Answer: Option D

34. For a 4-bit DAC, the least significant bit (LSB) is _____.

A.6.25% of full scale

B.0.625% of full scale

C.12% of full scale

D.1.2% of full scale

Answer: Option A

35. The dual-slope analog-to-digital converter finds extensive use in _____.

A.digital voltmeters

B.function generators

C.frequency counters

D.all of the above

Answer: Option D

36. The ADC0804 is an example of a _____.

A.single-slope analog-to-digital converter

B.dual-slope analog-to-digital converter

C.digital-ramp analog-to-digital converter

D.successive-approximation analog-to-digital converter

Answer: Option D

37. In a digital representation of voltages using an 8-bit binary code, how many values can be defined?

A.16

B.64

C.128

D.256

Answer: Option D

38. A 4-bit R/2R ladder digital-to-analog converter uses _____.

A.one resistor value

B.two resistor values

C.three resistor values

D.four resistor values

Answer: Option B

39. A binary-weighted-input digital-to-analog converter has a feedback resistor, Rf, of 12 k. If 50 A of current is through the resistor, voltage out of the circuit is _____.

A.0.6 V

B.–0.6 V

C.0.1 V

D.–0.1 V

Answer: Option B

40. The resolution of a 6-bit DAC is _____.

A.63%

B.64%

C.15.9%

D.1.59%

Answer: Option D

41. How are unwanted frequencies removed prior to digital conversion?

A.Pre-filters

B.Digital signal processing

C.Sample-and-hold circuits

D.All of the above

Answer: Option A

42. Which type of programming is typically used for digital signal processors?

A.Assembly language

B.Machine language

C.C

D.None of the above

Answer: Option A

43. Which of the following best defines Nyquist frequency?

A.The frequency of resonance for the filtering circuit

B.The second harmonic

C.The lower frequency limit of sampling

D.The highest frequency component of a given analog signal

Answer: Option D

44. Which is not an A/D conversion error?

A.Differential nonlinearity

B.Missing code

C.Incorrect code

D.Offset

Answer: Option A

45.Settling time is normally defined as the time it takes a DAC to settle within _____.

A.1/8 LSB of its final value when a change occurs in the input code

B.1/4 LSB of its final value when a change occurs in the input code

C.1/2 LSB of its final value when a change occurs in the input code

D.1 LSB of its final value when a change occurs in the input code

Answer: Option C

46.Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 MHz.

A.10.24 kHz

B.5 kHz

C.30.24 kHz

D.15 kHz

Answer: Option B

47. Which statement BEST describes the operation of a negative-edge-triggered D flip-flop?

A.The logic level at the D input is transferred to Q on NGT of CLK.

B.The Q output is ALWAYS identical to the CLK input if the D input is HIGH.

C.The Q output is ALWAYS identical to the D input when CLK = PGT.

D.The Q output is ALWAYS identical to the D input.

Answer: Option A

48. Propagation delay time, tPLH, is measured from the _____.

A.triggering edge of the clock pulse to the LOW-to-HIGH transition of the output

B.triggering edge of the clock pulse to the HIGH-to-LOW transition of the output

C.preset input to the LOW-to-HIGH transition of the output

D.clear input to the HIGH-to-LOW transition of the output

Answer: Option A

49. How is a J-K flip-flop made to toggle?

A.J = 0, K = 0

B.J = 1, K = 0

C.J = 0, K = 1

D.J = 1, K = 1

Answer: Option D

50. How many flip-flops are in the 7475 IC?

A.1

B.2

C.4

D.8

Answer: Option C

51. How many flip-flops are required to produce a divide-by-128 device?

A.1

B.4

C.6

D.7

Answer: Option D

52. The _____ circuit overcomes the problem of switching caused by jitter on the inputs.

A.astable multivibrator

B.monostable multivibrator

C.bistable multivibrator

D.Schmitt trigger

Answer: Option D

53. Why would a delay gate be needed for a digital circuit?

A.A delay gate is never needed.

B.to provide for setup times

C.to provide for hold times

D.to provide for setup times and hold times

Answer: Option D

54. An optocoupler is an integrated circuit with an LED and a zener diode encased in the same package.

A.True

B.False

Answer: Option B

55. A Schmitt trigger has VT+ = 2.0 V and VT– = 1.2 V. What is the hysteresis voltage of the Schmitt trigger?

A.0.4 volt

B.0.6 volt

C.0.8 volt

D.1.2 volts

Answer: Option C

56. Which of the following circuit parameters would be most likely to limit the maximum operating frequency of a flip-flop?

A.setup and hold time

B.clock pulse HIGH and LOW time

C.propagation delay time

D.clock transition time

Answer: Option C

57. What is the result of taking more samples during the quantization process?

A.More errors in the analog-to-digital conversion

B.More bit requirements

C.More accurate signal representation

D.More bit requirements and more accurate signal representation

Answer: Option D

58. Which A/D conversion method has a fixed conversion time?

A.Single-slope analog-to-digital converter

B.Dual-slope analog-to-digital converter

C.Digital-ramp analog-to-digital converter

D.Successive-approximation analog-to-digital converter

Answer: Option D

18. Which is a typical application of digital signal processing?

A.Noise elimination

B.Music signal processing

C.Image processing

D.All of the above

Answer: Option D

60. If a DAC has a full-scale, or maximum, output of 12 V and accuracy of 0.1%, then the maximum error for any output voltage is _____.

A.12 V

B.120 mV

C.12 mV

D.0 V

Answer: Option C

70. What do we call the manipulation of an analog signal in a digital domain?

A.Analog-to-digital conversion

B.Digital-to-analog conversion

C.Digital signal processing

D.Signal filtering

Answer: Option B

71. How many address bits are needed to select all memory locations in the 2118 16K × 1 RAM?

A.8

B.10

C.14

D.16

Answer: Option C

72. The check sum method of testing a ROM:

A.indicates if the data in more than one memory location is incorrect.

B.provides a means for locating and correcting data errors in specific memory locations.

C.allows data errors to be pinpointed to a specific memory location.

D.simply indicates that the contents of the ROM are incorrect.

Answer: Option D

73. Refer to the given figures (a) and (b). A logic analyzer is used to check the circuit in figure (a) and displays the waveforms shown in figure (b). The actual analyzer display shows all four data outputs, Q0-Q3. The analyzer's cursor is placed at position X and all four of the data output lines show a LOW level output. What is wrong, if anything, with the circuit?

A.Nothing is wrong, according to the display. The outputs are in the open state and should show zero output voltage.

B.The circuit is in the READ mode and the outputs, Q0-Q3, should reflect the contents of the memory at that address. The chip is defective; replace the chip.

C.The circuit is in the mode and should be writing the contents of the selected address to Q0–Q3.

D.The Q0–Q3 lines can be either LOW or HIGH, since the chip is in the tristate mode in which case their level is unpredictable.

Answer: Option D

74. What is the meaning of RAM, and what is its primary role?

A.Readily Available Memory; it is the first level of memory used by the computer in all of its operations.

B.Random Access Memory; it is memory that can be reached by any sub- system within a computer, and at any time.

C.Random Access Memory; it is the memory used for short-term temporary data storage within the computer.

D.Resettable Automatic Memory; it is memory that can be used and then automatically reset, or cleared, after being read from or written to.

Answer: Option C

75. The storage element for a static RAM is the _____.

A.diode

B.resistor

C.capacitor

D.flip-flop

Answer: Option D

76. In a DRAM, what is the state of R/W during a read operation?

A.Low

B.High

C.Hi-Z

D.None of the above

Answer: Option B

77. The condition occurring when two or more devices try to write data to a bus simultaneously is called _____.

A.address decoding

B.bus contention

C.bus collisions

D.address multiplexing

Answer: Option B

78. The difference between a PLA and a PAL is:

A.The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane.

B.The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane.

C.The PAL has more possible product terms than the PLA.

D.PALs and PLAs are the same thing.

Answer: Option A

79. ALM is the acronym for_____.

A.Array Logic Matrix

B.Arithmetic Logic Module

C.Asynchronous Local Modulator

D.Adaptive Logic Module

Answer: Option D

80. The GAL16V8 has:

A.16 dedicated inputs.

B.8 special function pins.

C.8 pins that are used as inputs or outputs.

D.All of the above

Answer: Option C

81. PALs tend to execute _____ logic.

A.SAP

B.SOP

C.PLA

D.SPD

Answer: Option B

82. How many pins are in an EDF10K70 package?

A.70

B.140

C.240

D.532

Answer: Option C

83. Convert hexadecimal value 16 to decimal.

A.2210

B.1610

C.1010

D.2010

Answer: Option A

84. Convert the following decimal number to 8-bit binary.

A.101110112

B.110111012

C.101111012

D.101111002

Answer: Option A

85. Convert binary 111111110010 to hexadecimal.

A.EE216

B.FF216

C.2FE16

D.FD216

Answer: Option B

86. Convert the following binary number to decimal.

010112

A.11

B.35

C.15

D.10

Answer: Option A

87. Convert the binary number 1001.00102 to decimal.

A.90.125

B.9.125

C.125

D.12.5

Answer: Option B

88. Decode the following ASCII message.

10100111010100101010110001001011001

01000001001000100000110100101000100

A.STUDYHARD

B.STUDY HARD

C.stydyhard

D.study hard

Answer: Option B

89. The voltages in digital electronics are continuously variable.

A.True

B.False

Answer: Option B

90. One hex digit is sometimes referred to as a(n):

A.byte

B.nibble

C.grouping

D.instruction

Answer: Option B

91.Which of the following is the most widely used alphanumeric code for computer input and output?

A.Gray

B.ASCII

C.Parity

D.EBCDIC

Answer: Option B

92. If a typical PC uses a 20-bit address code, how much memory can the CPU address?

A.20 MB

B.10 MB

C.1 MB

D.580 MB

Answer: Option C

93. Convert 59.7210 to BCD.

A.111011

B.01011001.01110010

C.1110.11

D.0101100101110010

Answer: Option B

94. Convert 8B3F16 to binary.

A.35647

B.011010

C.1011001111100011

D.1000101100111111

Answer: Option D

95. Which is typically the longest: bit, byte, nibble, word?

A.Bit

B.Byte

C.Nibble

D.Word

Answer: Option D

96. Assign the proper odd parity bit to the code 111001.

A.1111011

B.1111001

C.0111111

D.0011111

Answer: Option B

97. Convert decimal 64 to binary.

A.01010010

B.01000000

C.00110110

D.01001000

Answer: Option B

98. Convert hexadecimal value C1 to binary.

A.11000001

B.1000111

C.111000100

D.111000001

Answer: Option A

99. Convert the following octal number to decimal.

178

A.51

B.82

C.57

D.15

Answer: Option D

100. Convert the following binary number to octal.

0101111002

A.1728

B.2728

C.1748

D.2748

Answer: Option D